AD9361-CSH Data Sheet Revision

AD9361 CS DS Header (Rev. A vs Rev. B)

AD9361S-CSH REVA

AD9361S-CSH REVB

AD9361 Features

AD936S-CSH Rev A

FEATURES

- RF 2 × 2 transceiver with integrated 12-bit DACs and ADCs
- Transmit band: 46.875 MHz to 6.0 GHz
- Receive band: 70 MHz to 6.0 GHz
- Dual receivers: 6 differential or 12 single-ended inputs
- Superior receiver sensitivity with a NF of 2 dB at 800 MHz LO
- Receive gain control
  - Real-time monitor and control signals for manual gain
  - Independent AGC
- Dual transmitters: 4 differential outputs
- Highly linear broadband transmitter
  - Transmit EVM: −40 dB (typical) at 800 MHz
  - Transmit noise: −157 dBm/Hz (typical)
  - Transmit monitor: 66 dB dynamic range (typical) with 1 dB accuracy
- Integrated fractional-N synthesizers
  - 2.4 Hz typical LO frequency step size
- Multichip synchronization
- CMOS/LVDS digital interface

AD9361-CSH Rev B

FEATURES

- RF 2 × 2 transceiver with integrated 12-bit DACs and ADCs
- Transmit band: 46.875 MHz to 6.0 GHz
- Receive band: 70 MHz to 6.0 GHz
- Dual receivers: 6 differential
- Superior receiver sensitivity with a NF of 2 dB at 800 MHz LO
- Receive gain control
  - Real-time monitor and control signals for manual gain
  - Independent AGC
- Dual transmitters: 4 differential outputs
- Highly linear broadband transmitter
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- Integrated fractional-N synthesizers
  - 2.4 Hz typical LO frequency step size
- Multichip synchronization
- CMOS/LVDS digital interface

AD9361 General Description

AD9361S-CSH Rev A

GENERAL DESCRIPTION

The AD9361S-CSH is a high performance, highly integrated, RF agile transceiver designed for use in 3G and 4G applications. Its programmability and wideband capability make it ideal for a broad range of transceiver applications. The device combines an RF front end with a flexible mixed-signal baseband section and integrated frequency synthesizers, simplifying design-in by providing a configurable digital interface to a processor. The AD9361S-CSH receiver LO operates from 70 MHz to 6.0 GHz and the transmitter LO operates from 46.875 MHz to 6.0 GHz range, covering most licensed and unlicensed bands. Channel bandwidths from less than 200 kHz to 56 MHz are supported.

AD9361-CSH Rev B

GENERAL DESCRIPTION

The AD9361-CSH is a high performance, highly integrated, RF agile transceiver designed for use in 3G and 4G applications. Its programmability and wideband capability make it ideal for a broad range of transceiver applications. The device combines an RF front end with a flexible mixed-signal baseband section and integrated frequency synthesizers, simplifying design-in by providing a configurable digital interface to a processor. The AD9361-CSH receiver LO operates from 70 MHz to 6.0 GHz and the transmitter LO operates from 46.875 MHz to 6.0 GHz range, covering most licensed and unlicensed bands. Channel bandwidths from less than 200 kHz to 56 MHz are supported.

AD9361 CS Features

AD9361S-CSH Rev A

COMMERCIAL SPACE FEATURES

- Supports aerospace applications
- Certificate of Conformance
- Wafer diffusion lot traceability
- Qualification based on flows per NASA PEM-INST-001 and SAE AS6294
- Burn-in, life test, and deltas analysis
- Radiation lot acceptance test (RLAT)
  - Total ionizing dose (TID)
- Radiation benchmark
  - Single event latchup (SEL)
- Outgassing characterization

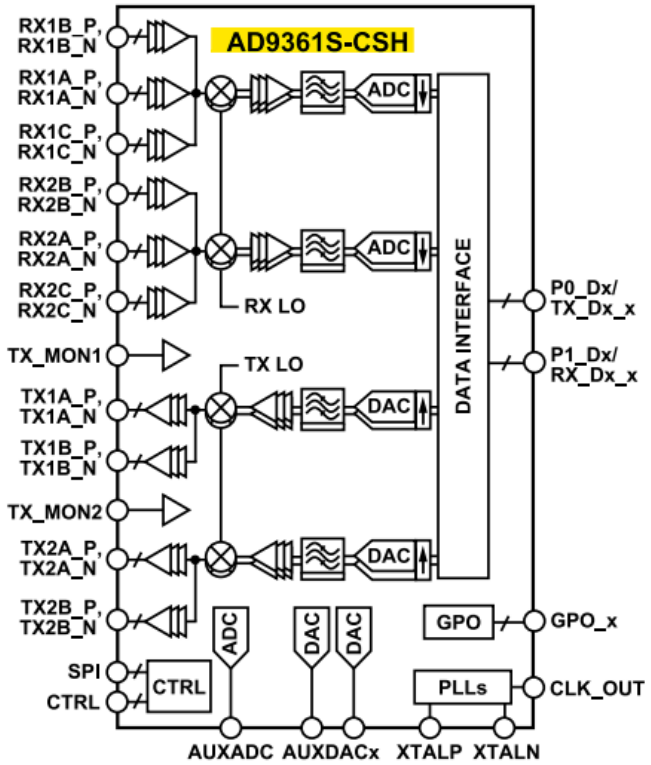
AD9361-CSH Rev B

COMMERCIAL SPACE FEATURES

- Supports aerospace applications
- Certificate of Conformance
- Wafer diffusion lot traceability
- Qualification based on flows per NASA PEM-INST-001 and SAE AS6294
- Burn-in, life test, and deltas analysis
- Radiation lot acceptance test (RLAT)
  - Total ionizing dose (TID)
- Radiation benchmark
  - No single event latch-up (SEL) occurs at effective linear energy transfer (LET): ≤80 MeV-cm^2/mg
- Outgassing characterization

AD9361 Figure 1

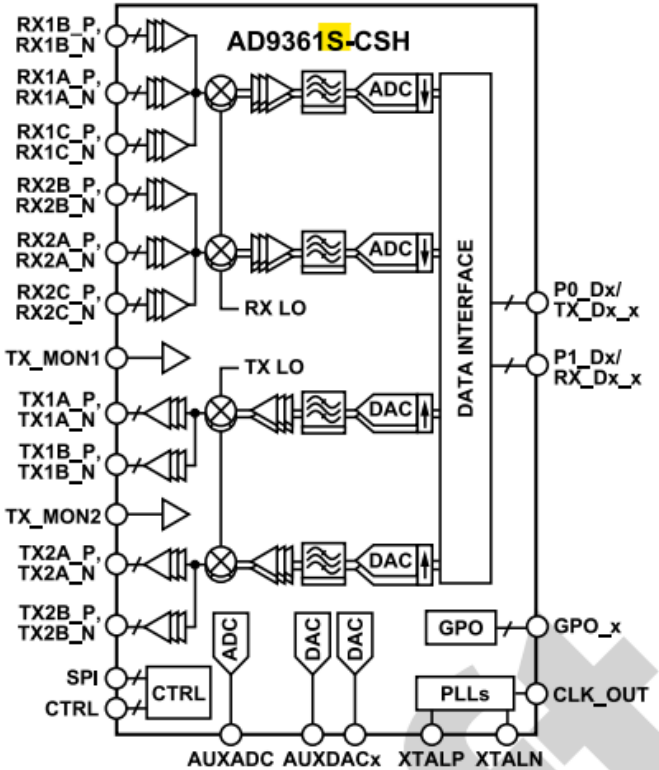
AD9361S-CSH Rev A



NOTES
1. SPI, CTRL, P0_Dx/TX_Dx_x, P1_Dx/RX_Dx_x, AND GPO_x CONTAIN MULTIPLE PINS.

Figure 1.

AD9361-CSH Rev B



NOTES
1. SPI, CTRL, P0_Dx/TX_Dx_x, P1_Dx/RX_Dx_x, AND GPO_x CONTAIN MULTIPLE PINS.

Figure 1. Functional Block Diagram

AD9361 Specs Table

AD9361S-CSH Rev A

Table 1. (Continued)

Parameter[1]	Symbol	Min	Typ	Max	Unit	Test Conditions/ Comments
REFERENCE CLOCK						The reference clock is either the input to the XTALP/XTALN pins or a line directly to the XTALN pin
Input						
Frequency Range		19		50	MHz	Crystal input
		10		80	MHz	External oscillator
Signal Level			1.3		V p-p	AC-coupled external oscillator

AD9361-CSH Rev B

Table 1. (Continued)

Parameter[1]	Symbol	Min	Typ	Max	Unit	Test Conditions/ Comments
REFERENCE CLOCK						The reference clock is either the input to the XTALP/XTALN pins or a line directly to the XTALN pin
Input						
Frequency Range		19		50	MHz	Crystal input
		20		80	MHz	External oscillator
Signal Level		0.8		1.3	V p-p	AC-coupled external oscillator. Larger swings close to max level give best performance.

AD9361 Burn-in Table description

AD9361S-CSH Rev A

LIFE TEST AND BURN-IN DELTA LIMITS SPECIFICATIONS

Electrical characteristics at VDD_GPO = 3.3 V, VDD_INTERFACE = 1.8 V, VDDD1P3_DIG = 1.3 V, and all other VDDA1P3_x pins = 1.3 V. Deltas are performed at T_A = 25°C. Burn-in oven temperature at T_A = 110°C, unless otherwise noted.

Table 11.

Parameter	Min	Typ	Max	Unit
SUPPLY CHARACTERISTICS				
Total Sleep Mode Current	−3		+3	mA
DIGITAL INPUT CURRENTS				
Low	−60		+60	nA
High	−60		+60	nA
TRANSMITTERS, 2.3 GHz				
Fundamental Output Power	−1.5		+1.5	dBm

AD9361-CSH Rev B

LIFE TEST AND BURN-IN DELTA LIMITS SPECIFICATIONS

Electrical characteristics at VDD_GPO = 3.3 V, VDD_INTERFACE = 1.8 V, VDDD1P3_DIG = 1.3 V, and all other VDDA1P3_x pins = 1.3 V. Deltas are performed at T_A = 25°C.

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TRANSMITTERS, 2.3 GHz				

SPECIFICATIONS

Table 11. (Continued)

Parameter	Min	Typ	Max	Unit
Fundamental Output Power	−1.5		+1.5	dBm

AD9361 Radiation Features Table

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RADIATION FEATURES

Table 16. Radiation Features

Specifications	Value	Unit
Maximum Total Dose Available (Dose Rate = 50 rad(Si)/s to 300 rad(Si)/s)[1]	100	krad(Si)
No Single Event Latch-Up (SEL) Occurs at Effective Linear Energy Transfer (LET)[2]	≤80	MeV-cm^2/mg

1 Guaranteed by device and process characterization. Contact Analog Devices for data available up to 100 krads.

2 Limits are characterized at initial qualification and after any design or process changes that may affect the SEL characteristics, but are not production lot tested unless specified by the customer through the purchase order or contract. For more information on single event effect (SEE) test results, contact Analog Devices for further data beyond published report on the Analog Devices website.

AHEAD OF WHAT'S POSSIBLE

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